R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENTS

Although Applicant's representative does not necessarily agree with the position taken in the Office Action that the claimed "first predetermined condition" and the "second predetermined condition" could not be discerned by a person of ordinary skill in the art when read in light of the specification (see page 2, line 13 through page 3, line 12 of the Office Action), the phrases "first predetermined condition" and the "second predetermined condition" have been replaced with the phrases "said multiple chroma picture requests" and "said multiple luma picture requests", respectively in light of the Examiner's comments. Support for the claim amendments can be found in the drawings as originally filed, for example, in FIG. 27, and in the specification as originally filed, for example, on page 30, lines 3-15. As such, no new matter has been introduced.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1, 2, 4-16 and 18-22 under 35 U.S.C. §103(a) as being unpatentable over Yasuki et al. (U.S. Patent No. 5,712,689; hereinafter Yasuki) in view of Cahill, III et al. (U.S. Patent No. 5,784,047; hereinafter Cahill) is respectfully traversed and should be withdrawn.

The rejection of claims 3 and 17 under 35 U.S.C. §103(a) as being unpatentable over Yasuki in view of Cahill, and further in view of Malinowski et al. (U.S. Patent No. 5,574,572; hereinafter Malinowski) is respectfully traversed and should be withdrawn.

Yasuki is directed to a digital television set (Title of Yasuki). Cahill is directed to a method and apparatus for a display scaler (Title of Cahill). Malinowski is directed to a video scaling method and device (Title of Malinowski).

In contrast to the cited references, the presently claimed invention (claim 1) provides an address generator circuit configured to generate one or more first control signals, wherein the address generator circuit comprises a finite state machine configured to allow multiple luma picture requests and multiple chroma picture requests to follow in sequence and the finite state machine provides (i) an idle after chroma state configured to move to a chroma state in response to the multiple chroma picture requests and (ii) an idle after luma state configured to move to a luma state in response to the multiple luma picture requests. Claims 15 and 16 include similar limitations. Yasuki and Cahill do not teach or suggest all the elements of the presently claimed invention. As such, the presently claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

Specifically, the Office Action admits that "Cahill, III et al. does not teach the limitation of a finite state machine configured to allow multiple luma and multiple chroma requests to

follow in sequence" (see page 12, lines 18-19 of the Office Action).

Yasuki does not cure the deficiency of Cahill. Assuming, *arguendo*, the DMA device 384 in FIG. 5 of Yasuki is similar to the presently claimed address generator circuit and the state machine 385 in FIG. 5 of Yasuki is similar to the presently claimed finite state machine (as suggested on page 8 of the Office Action and for which Applicant's representative does not necessarily agree), the Office Action does not appear to have met the Office's burden to factually establish that Yasuki teaches or suggests an address generator circuit as presently claimed. Specifically, the Office Action does not present any objective evidence or convincing line of reasoning why an artisan with an ordinary level of skill in the field of the invention would consider the state machine 385 as being a part of the DMA device 384. For example, the state machine 385 is shown as a separate box external to the DMA device 384. Since the state machine 385 is shown as a separate box external to the DMA device 384 one of ordinary skill in the art would not consider the DMA device 384 as **comprising** the state machine 385. Therefore, the Office Action fails to establish a factual basis to support a *prima facie* conclusion of obviousness. As such, the rejection does not appear to be sustainable and should be withdrawn.

Furthermore, assuming, *arguendo*, the state machine 385 in FIG. 5 of Yasuki is similar to the presently claimed finite state machine (as suggested on page 8, lines 11-16 of the Office Action

and for which Applicant's representative does not necessarily agree), Yasuki does not teach or suggest that the state machine 385 necessarily has (i) an idle after chroma state configured to move to a chroma state in response to multiple chroma picture requests and (ii) an idle after luma state configured to move to a luma state in response to multiple luma picture requests, as presently claimed. In particular, one of ordinary skill in the art would understand that a finite state machine is defined by describing a set of possible states and the transitions between the states (e.g., such as the state diagram shown in FIG. 27 of the Specification) (see definition of finite state machine from Laplante, Comprehensive Dictionary of Electrical Engineering, pp 249-250, submitted previously with the Amendment filed October 12, 2004 and attached as Exhibit A). Yasuki does not disclose a state diagram for the state machine 385. The only statement contained in Yasuki regarding the state machine 385 reads:

> The bus controller 338 is composed of a bus control section 381 which checks the signal of the data transfer, a bus arbiter section 382 which controls the competition of the bus with CPU 337, an interrupt handling section 383, DMA (direct memory access device) 384 used for the data transfer, and **a state machine 385 which controls the bus controller 338 and the overall system** (Column 7, lines 46-52 of Yasuki, emphasis added).

Yasuki is silent regarding what specific states are provided by the state machine 385 or how the state machine 385 transitions between such states. Since Yasuki is silent regarding the state machine 385 providing (i) an idle after chroma state configured to move to

a chroma state in response to multiple chroma picture requests and (ii) an idle after luma state configured to move to a luma state in response to multiple luma picture requests as presently claimed, it follows that Yasuki does not teach or suggest a finite state machine as presently claimed. Therefore, Yasuki and Cahill do not teach or suggest each and every element of the presently claimed invention. As such, the presently claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

Furthermore, the Office Action fails to provide any objective evidence or a convincing line of reasoning why a person of ordinary skill in the field of the invention would consider Yasuki to teach or suggest a finite state machine necessarily configured to allow multiple luma picture requests and multiple chroma picture requests to follow in sequence as presently claimed. Yasuki states that:

> The image data from FIFO memories 369,457 and 458 are selected by the bus controller 338 and supplied to the vertical processing circuit 334 time-divisionally via the selector 459. **That is, each image data is transferred time-divisionally in a predetermined time unit via the bus 333, therefore the transfer of each image data does not compete.** Furthermore, the image data based on a plurality of images is input to the bus 333, however, if it is compressed in the horizontal direction, the number of pixels are reduced, whereby it is not caused to exceed the transfer capacity of the bus 333. (Column 13, lines 10-20 of Yasuki, emphasis added by Applicant's representative).

A person of ordinary skill in the art would not understand the transfer of image data time-divisionally as mentioned in Yasuki to necessarily require that the image data be transferred through multiple chroma picture requests and multiple luma picture requests following in sequence as presently claimed. Furthermore, the Office Action states that Yasuki is silent regarding switching or alternating between requests (see page 4, lines 6-11 of the Office Action). Yasuki is equally silent regarding multiple chroma picture requests and multiple luma picture requests following in sequence, as presently claimed. Although a prior art device "may be capable of being modified to run the way the apparatus is claimed, there must be a suggestion or motivation in the reference to do so" (see MPEP §2143.01(III)). Yasuki does not provide such a suggestion or motivation. Rather, the Office Action appears to be using only what the Applicant has taught. Therefore, the Office Action does not appear to have met the Office's burden to establish a factual basis to support a *prima facie* conclusion of obviousness. As such, the presently claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

Furthermore, assuming, *arguendo*, the state machine 385 in FIG. 5 of Yasuki is similar to the presently claimed finite state machine (as suggested on page 8, lines 11-16 of the Office Action and for which Applicant's representative does not necessarily agree), the Office Action does not present any objective evidence or convincing line of reasoning why a person of ordinary skill in the art would consider the interrupt signal IREQ 1 of Yasuki or the

bus request signals REQ and BUS-REQ of Yasuki as necessarily being the same as the presently claimed multiple chroma picture requests and multiple luma picture requests. Specifically, Yasuki states:

> **The bus control section 381 issues a bus request signal (REQ) for requesting the bus use based on FIFO empty and FIFO full** showing the empty state of the FIFO memory of the device which sends data to the bus 333 and the device which is supplied data from the bus 333. And the bus control section 381 sends data based on ACK to the bus arbiter section 382, when the bus acknowledge signal (BUS-ACK) showing the acknowledgment of the bus use is given from CPU 337. **The interrupt handling section 383 issues a bus request signal (BUS-REQ) to CPU 337, when the interrupt signal (IREQ1) showing the request for data transfer based on the processing completion** is given from the horizontal processing circuit 332, and sends the data based on this BUS-ACK to the bus arbiter section 382, when the bus acknowledge signal (BUS-ACK) is given from CPU 337 (column 7, lines 53-67 of Yasuki, emphasis added by Applicant's representative).

Thus, Yasuki associates the bus request signal REQ with the fill status of FIFOs rather than either luma or chroma picture requests. Yasuki further associates the signals IREQ 1 and BUS-REQ with the completion of horizontal processing rather than either luma picture requests or chroma picture requests. A person of ordinary skill in the art would not consider signals associated with the fill status of a FIFO or the completion of horizontal processing to be the same as the luma picture requests or chroma picture requests as presently claimed. Therefore, the Office Action fails to establish a factual basis to support a *prima facie* conclusion of obviousness.

As such, the rejection does not appear to be sustainable and should be withdrawn.

Claims 2-14 and 17-22 depend, directly or indirectly, from either claim 1 or claim 16 which are believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

Furthermore, with respect to claims 21 and 22, the Office Action does not apply the references to the specifically claimed limitations. For example, claim 21 recites "The apparatus according to claim 1, wherein said idle after chroma state is further configured to move to any of (i) said luma state, (ii) a BTMP after luma state, (iii) an SPU/VBI state, (iv) said idle after luma state, and (v) said chroma state." Claim 22 recites "The apparatus according to claim 1, wherein said idle after luma state is further configured to move to any of (i) said chroma state, (ii) a BTMP after chroma state, (iii) an SPU/VBI state, (iv) said luma state and (v) said idle after chroma state." The Office Action states "said luma state (Y of num. 452 is moved to the next stage, fig. 12, num. 460)" (see page 20, lines 1-7 of the Office Action). The reference to data moving from one STAGE (num. 452 of Yasuki) of a circuit to another STAGE (num. 460 of Yasuki) of a circuit does not address whether the state machine 385 has (a) an idle after chroma **STATE** that is further configured to move to any of (i) said luma **STATE**, (ii) a BTMP after luma **STATE**, (iii) an SPU/VBI **STATE**, (iv) said idle after luma **STATE**, and (v) said chroma **STATE** or (b)

an idle after luma **STATE** is further configured to move to any of (i) said chroma **STATE**, (ii) a BTMP after chroma **STATE**, (iii) an SPU/VBI **STATE**, (iv) said luma **STATE** and (v) said idle after chroma **STATE**, as presently claimed. Therefore, the Office Action does not appear to meet the Office's burden to establish a factual basis to support a *prima facie* conclusion of obviousness with respect to claims 21 and 22. Therefore, the rejection of claims 21 and 22 do not appear to be sustainable and should be withdrawn.

SHOWING UNDER 37 CFR 1.116(b)

The amendments presented herein should be admitted because the amendments made comply with a requirement of form expressly set forth in the Office Action (see 37 CFR 1.116(b)(1)). Specifically, the Office Action states:

> Both the claimed "first predetermined condition" and the "second predetermined condition" is not given any patentable weight and ought to be deleted **or amend the claimed "first predetermined condition" and the "second predetermined condition" so that the amendment will correspond with the specification.** (see page 3, lines 1-4 of the Office Action, emphasis added by Applicant's representative).

The Office Action further states:

> For example, page 30, lines 3-15 include the use of a request which may correspond to the claimed "first predetermined condition" and the "second predetermined condition." Thus, claim 1 should include (i) an idle after chroma state configured to move to a chroma state in response to a first **request** and (ii) an idle after luma state configured to move to a luma state in response to a second **request.** (see

> page 3, lines 5-9 of the Office Action, emphasis by the Examiner).

Therefore, the amendments presented herein comply with a requirement of form expressly set forth in the Office Action and should be admitted under 37 CFR 1.116(b)(1).

Furthermore, the amendments should be admitted under 37 CFR 1.116(b)(2) as presenting the claims in better form for consideration on appeal based on the statements made in the Office Action. In particular, the Office Action states that:

> The claimed "first predetermined condition" and the "second predetermined condition" could not be discerned on page 30, lines 3-15 or in combination with any other part of the specification (see page 3, lines 10-12 of the Office Action.

However, the Office Action admits that:

> . . . page 30, lines 3-15 include the use of a request which may correspond to the claimed "first predetermined condition" and the "second predetermined condition" (see page 3, lines 5-7 of the Office Action).

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicant's representative between the hours of 9 a.m. and 5 p.m. ET at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

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